ECE 764 Lab 3 - Introduction to Microstrip Circuits
Due Monday, March 18, 2019
(Part I due by Spring Break)

Purpose

This lab is intended to familiarize you with designing, building, and testing microwave circuits on PC boards - in preparation for the upcoming radar project. You will be introduced to Keysight's ADS software that will be used extensively in the project design phase. You will also learn some important issues with board design including parasitic inductances of vias and capacitances of PC board traces. While often a problem, these parasitics can be embraced to form bandpass filters, which you will design and test. Finally, you will build and test microwave amplifiers to learn about circuit board layout, surface-mount construction techniques, S-parameter measurement using vector network analyzers (VNAs), and some important system design issues such as amplifier compression points and stability.

Lab Overview

Circuits and issues to be studied in this lab include:

- Simulations of PC board vias and traces to estimate values of inductive and capacitive parasitics.
- Design of microwave bandpass filters using these parasitic elements.
- Use of lambda/4 bias-decoupling lines in amplifier circuits.
- ~~Single-stub and lambda/4 impedance-transformer based matching networks (simulation only).~~
- Building amplifier boards to learn about PC board design and construction techniques.
- Using "cal kits" and reference planes when measuring S-parameters of amplifiers and filters.
- Measuring the cascaded response of amplifiers and filters.
- Effectiveness of bandpass filters and attenuation "pads" to mitigate excess low-frequency gain and potential stability problems in amplifier cascades.

Teams

As before, this lab is constructed for teams of two persons. You can split the workload in the writeup as in the previous project. However, you are strongly encouraged to work closely together, and each person should participate in all parts so that you learn what you need to do the upcoming project and to be successful in your careers. To help guarantee this, each of you will design and test your own unique amplifier and filter and then cascade your circuit with your partner's to achieve higher gain and (hopefully) a good filter response function.

Operating Frequencies

In the project we will have circuits operating around 1.9 and 5.8 GHz. Therefore, this lab is designed to help you understand realizable gains and other issues at these frequencies. Because these frequencies are roughly an order of magnitude higher than those used in Lab 2, you should "think small" ;-) That is, you will need to understand that circuit dimensions will easily be larger than lambda/20 and that will need to embrace transmission-line theory everywhere !

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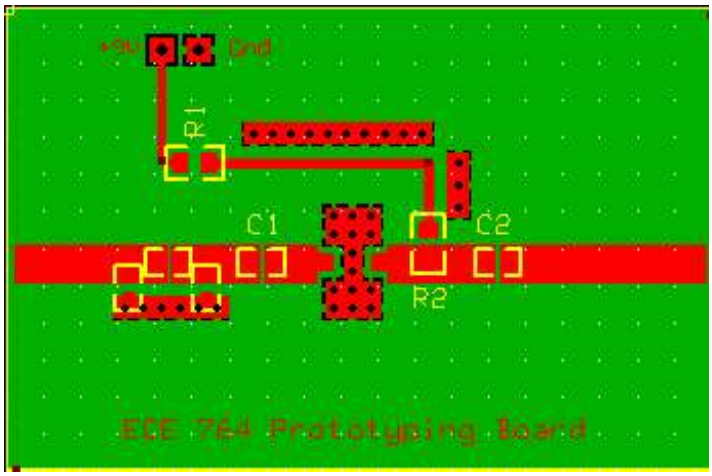
PC Boards and Amplifiers

For this lab you will work with pre-designed boards and populate them with various amplifiers and associated biasing components from your kit and lab stock. The boards are expected to be available by the end of the week (March 1). They use a "62 mil" (i.e. 0.062 in or 1.6 mm) thick double-sided "FR4" (fire-retardant fiberglass-epoxy) single-ply substrate with a solid ground plane on the back side. All components will be soldered on the top side. Connections to test equipment will be through female SMA end-launch connectors.

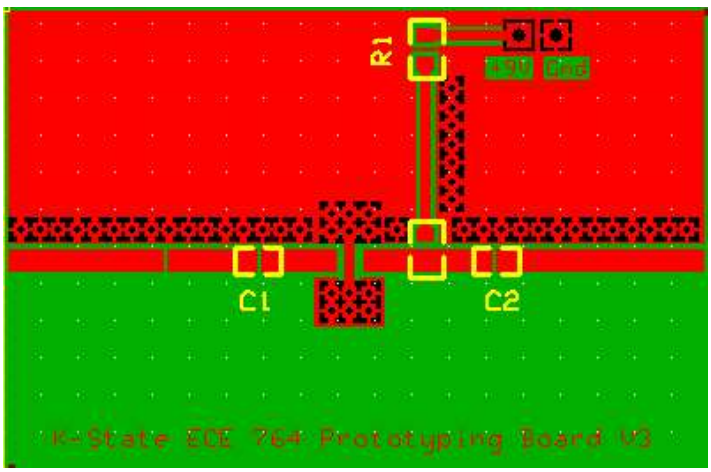
Locate the amplifiers in your individual kits (LEE-39+, or GALI-1) and study their datasheets.
Pictures of the PC boards on which you will build your amplifier circuit are shown below.

Each person on a team must chose a different amplifier AND a different board.
The first option uses typical "microstrip" with lines sized for 50 Ohm characteristic impedance. The second uses a variant of "coplanar-waveguide" (CPW). This variant is called single-sided CPW (SS-CPW) and was pioneered at K-State in a previous ECE764 class. Due to its "flanking" ground, it allows more narrow traces and has better performance in general. Some information on it's design and advantages can be found in a recent research paper at: https://ieeexplore.ieee.org/document/8534266 (also posted on our class website).

Traditional Microstrip board



Single-sided CPW board



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Lab Instructions

The sections below give an outline of what you should do and document in this lab. Additional details for some parts (e.g. using ADS, building circuits, and operating the VNA equipment) will be presented in class. ***As always, take pictures and printouts*** while you do the lab for use in the writeup, and if you are not sure what to do or how to do something, ask someone.

Part I Layout and Component Parasitics at Microwave Frequencies

At high frequencies, wires can no longer be treated as simple nodes. When their length exceeds more than about 1/20th of a wavelength (e.g. about 1 mm at 5.8 GHz for $v_p = 0.5c$), the phase shifts from one end of a connection to the other are significant enough that they cannot be ignored. In this case, distributed inductance and capacitance is present and can be modeled using transmission-line theory, as we are discussing in class.

In some special cases however, one can sometimes model effects more simply, taking account of "parasitic" inductance of a grounded trace or via, or the parasitic capacitance of an open trace. This part of the lab investigates some of these issues using the ADS simulator.

Do the following first with traditional Microstrip, and then try to assess the same issues by doing again using CPW. Each teammember should try one of these approaches.
Note that ADS does not have SS-CPW, but if you use normal CPW with about double the distance between the trace and ground-flank, it should approximate SS-CPW reasonably well (why?). Use a 10 mil separation between trace and ground flank in CPW for this.

1. Behavior of ground connections at microwave frequencies

i. Read the handout on operation of ADS and then create a schematic, placing a short (500 mil = 0.5 inch) length of trace on it, with the right-side end connected to ground. Use the MLIN element from the ADS TLines-Microstrip menu (or CPWG from TLines-Microstrip menu as appropriate) and the ground symbol from the top menu bar.
ii. Enter a width value of 10 mil and a length of 500 mil for the PC board trace modeled by the MLIN element (Use 10 mil for gap on the CPW line).
iii. Place an "MSUB" item from the TLines-Microstrip menu (or "CPWSUB" from TLines-Waveguide menu, as appropriate) and configure it with the parameters of our PC board material and copper traces: (H=62 mil, Er=4.6, TanD=0.01, Cond=6E7, and T= 1mil).
iv. Switch to the Simulation-S_Param menu and place a Term (with ground) on the left end of the MLIN, and an "SP" simulation setup item anywhere on the schematic. The Term item acts as a 50 Ohm source or load and will be used to emulate measurements made with a network analyzer. Edit the simulation setup item to sweep from 10 MHz to 10 GHz, with a step size of 10 MHz.
v. Print out a readable copy of your resulting schematic to include in your writeup
vi. Run the simulation using the Gear icon on the top menu bar and plot the result by placing a Smith Chart item in the resulting display window and selecting "S(1,1)" to plot.
vii. Place markers at the lowest, middle, and highest frequencies, and print out the result. Notice the curve begins near Z = 0 as one would expect for a grounded trace at 1MHz, where the line is much shorter than a wavelength. At higher frequencies, the impedance is of the form Z = 0 + j X, which is inductive, and it eventually wraps

around to an open-circuit on the right and then into the capacitive region of the chart past about 3.4 GHz, and back to inductive if you go past about 7 Ghz (for this ½ inch line).

viii. Note that below the frequency where Z = 0 + j50, the impedance is roughly proportional to frequency, so that this shorted line can be modeled to first-order as an inductance to ground at this lower frequency range. Place additional markers to find the frequencies where the Z value is +j 50, where it is + j 25, and where it is + j 12.5 to verify this. Is the reactance reasonably proportional to frequency? Be sure your markers are on the correct 'loop' ! (the outer-most one that is the lower frequency region)

ix. Use these values to estimate the inductance of the wire. What is this approximate inductance per unit length implied ? Does it agree with the often used estimates of 0.25 to 1 nH/mm or 5 to 20 nH / inch ?

x. Modify the trace to be 100 mils wide and repeat to determine the inductance per unit length. How does width of the trace affect the low-frequency inductance (for each type of line) ?

xi. At a sufficiently high frequency, the impedance of a grounded trace actually becomes an *open circuit*. Find this frequency by placing a marker at the Z=infinity point on the chart (right side) and use it to estimate the velocity of propagation on the 100 mil x 500 mil line. (Recall that it should become an open circuit when the length of the line is lambda / 4). Find the velocity of propagation expressed as a percent of the velocity of light c.

2. Behavior of vias to ground at Microwave frequencies

One difficulty we will need to deal with when building our radars, especially if we use 1/16" thick FR4 board and traditional microstrip trace design, is the fact that the vias needed to make connection to the back-side ground plane will show significant parasitic inductive behavior. For example, the ground pin on our amplifiers will not really be truely at (backside-board) ground. It will be separated from this ground by an inductive connection through the via (as well as its physical pin). In this part, we will estimate how large this inductive impedance may be at your chosen frequency when using Microstrip design and then look at some solutions to the problem. You do not need to do this part with the CPW line type for reasons mentioned below, and the fact that the ADS simulator doesn't do CPW well anyway. We should really be using the 3D simulator for that...

i. Replace the ground symbol on the right side of your schematic with a VIAGND item from the TLines-Microstrip menu.

ii. Edit the MLIN to make it only 5 mils long (effectively 0), so that we will be simulating essentially only the via's inductance. Print the resulting schematic.

iii. Simulate and use markers to find the complex impedance and then the inductance of the via. Print the resulting Smith Chart and write the inductive reactance in Ohms and the implied inductance on it.

iv. Since this value is non-trivial relative to the signal impedances (50 Ohm source and load values) elsewhere in our circuit, microwave engineers often use multiple vias (as well as multiple ground pins on the ICs). Add a second VIAGND in parallel, but connect it to the first one using a short MLIN to model that it is not physically in the same location. Use a 50 mil wide line with a 25 mil length to represent a realistic distance given the hole sizes in the via.

v. Simulate and comment on how much it lowered the inductive parasitics in the ground-via connection. Why is it not half of the previous value?

vi. Examine the microstrip amplifier board on page 2 and note that 7 vias are used on each of the two amplifier ground pins. Estimate what the net inductive parasitic impedance would be in this case. (Don't sim. Just reason through it to arrive at an educated guess. Sims are great - but they don't provide as much insight as actual thinking. The best practice is to think through first and then sim as necessary to check your reasoning)

Note that the problem of "via-to-ground" inductance largely goes away when CPW (or SS-CPW) is used, since the ground is available on the top side of the board in the form of the ground-flank(s) on the CPW. The amplifier's ground pin is soldered to this ground flank directly in the SS-CPW board. This is a major advantage of CPW in general !

3. Behavior of open-circuit "stubs" on PC boards

Just as a shorted line acts as an inductance and can become an open, an open line can act as a capacitance and become a short at sufficiently high frequency. In this part, we will just look at the effects. Later, we will use this to make simple LC bandpass filters in our experiments and possibly in our radars.

i. Remove the vias from the previous Microstrip schematic and restore the original trace to its 500 mil length (with 100 mil width).
ii. Simulate the resulting open-circuit line and find the capacitance per unit length and propagation velocity implied in the results. Explain how you did this and print your schematic and Smith chart results to back-up your estimates.

Part II Designing and simulating microstrip circuits

Most microwave amplifiers are designed to have close to 50 Ohm input and output impedances so that they can use 50 Ohm transmission lines to connect to other circuits, avoiding the need to deal with impedance transformations caused by the connections. While such amplifiers purchased commercially are typically "well-matched", user-designed matching networks can sometimes be useful to achieve somewhat higher gains.

Since modern amps are usually matched (to 50 Ohms) in today's world, we will go over this topic in class, but not do it here. Instead, we will concentrate on the basics of biasing, decoupling, and DC-blocking in amplifiers, and on their performance in terms of the maximum power levels our amps can be used at. This will be needed when you do your radar designs. We will also look at some simple bandpass filter designs techniques.

1. Simulating amplifiers and effects of bias lines and DC blocking capacitors

i. To simulate your amplifier, create a new ADS schematic using an S2P item from the Data Items menu, adding a 50 Ohm Term on both the input and the output. Download the S-parameter model file for your amplifier from Minicircuits or our class webpage and set the File parameter to point to the S2P model file.
ii. Simulate from 100 MHz to 10 GHz (without any MLIN or CPWG traces at input or output) to verify the S11 and S21 (input impedance and gain) in the datasheet. Just plot dB graphs, not Smith charts. Compare with your device's datasheet.
iii. Modify your schematic by adding an AC-grounded lambda/4 bias decoupling line at the amplifier output pin as discussed in class and included in the PCB layouts on page 2. Such lines can be used to supply Vdd power to the device while preventing the output signal from being loaded down by the bypassed supply connection. The lambda/4 decoupling line should be a simple 10 mil wide MLIN (CPWG) trace with electrical-length of lambda/4 at your operating frequency. Place a capacitor at the end of the line opposite the amplifier to create the AC ground. Calculate and use a reasonable standard-value capacitance that will have an impedance of < 0.1 Ohm at your targeted operating frequency. IMPORTANT: Adjust the "lambda/4" line's length as needed to account for the via inductance (if any) and for the length of an 0603 size (60 x 30 mil) capacitor and its pads.
iv. Next, add DC blocks (AC coupling caps) at the input and output. Calculate and use reasonable standard-value capacitances that will have an impedance of about 1 Ohm at your targeted operating frequency. Ideally you should add 60 mil long by 30 mil wide MLIN traces to model the "impedance-bumps" the capacitors create (since they are not as wide or as close to the ground-plane as the 50 Ohm transmission line and will therefore

have a higher Zo value than 50 Ohms). But leave those off for now, since they could muddy the results for the sims below...

v. Simulate S22 from 100 MHz to 10 GHz and verify the output return loss is OK at your frequency. It might not be if you messed up on the length of the AC-grounded lambda/4 bias decoupling line !

vi. Simulate S21 from 100 MHz to 10 GHz and confirm the gain *at your targeted frequency* is not significantly changed from the datasheet and simulation values before the bias line and coupling capacitors were added. Why is the gain now less than before at other frequencies? (There may be multiple reasons).

vii. When you have it working, print your schematic and your S21 and S22 plots. Why is S22 worse at lower and higher frequencies than in the datasheet ?

2. Designing and Simulating Bandpass Filters

i. Using the techniques discussed in class, design a one or two pole bandpass filter at your chosen frequency, with a fractional bandwidth of about 20 %. The designs should be different for the two different boards!

ii. Create a schematic of your filter in Agilent ADS. Simulate it alone (with Terms on both the input and the output) and refine it until the center frequency and bandwidth are correct to within about 10 percent, the shape is good, the insertion loss is reasonable, and the in-band input and output return loss values are at least 10 dB. Be sure to use appropriate "microstrip T's" to account for the stubs merging into the main line.

iii. Print/plot your final filter's schematic and response plot(s).

iv. Add the filter to the ***input*** side of your amplifier and simulate the composite design. Plot and comment on S21. Does the filter help reduce gain at the frequencies outside of your chosen frequency? In particular, does it help to reduce low-frequency gain ?

Part III Measurement of Amplifier Parameters

In this last part, you will gain experience in building an amplifier and characterizing its performance. The construction of your amp will help you with design/layout decisions when you are called to make your own circuit boards in the project. The data you collect will help you in making choices on which amplifiers to use in your radar designs and whether or not to add filters and/or attenuation "pads" to improve stability. More details will be provided in the coming week while the circuit boards are being sent out for fab, but here is a brief outline.

1. Biasing and Construction

i. Decide how you want to configure the bias circuits per discussions in class. Assume a 9V DC supply (since that is what we will design for in the project) and see the device datasheet for your amp for more information on the current and voltage needed at the output pin in order to calculate a biasing resistance value.

ii. Solder the main components on your board, including the bias resistor and decoupling line capacitor, the DC blocking capacitors, the amp itself, the power-supply connection header pins, and the microwave SMA connectors.

2. Scalar Insertion Gain Measurements using Signal Generator and Spectrum Analyzer

i. Use the test equipment on the side of the lab opposite the window, where the X and Ku-Band benches are.

ii. Connect your board to a power supply with the supply off and the voltage knob turned all the way down (CCW). Using the signal generator, supply an RF input signal at your design frequency (5.8 GHz).. IMPORTANT: You should input a reasonably low level RF signal (e.g. -20 dBm) since the amplifier will not show the proper gain (and could even be damaged) if the input signal is too high, causing the output to saturate.

iii. Connect the output of the amplifier to a spectrum analyzer.

iv. Slowly increase the DC supply voltage toward 9V while monitoring the current. Verify the amplifier draws a reasonable amount of current. Stop and fix if the current exceeds 50 mA, which could be enough to damage it.

v. Check to see if the circuit is stable. That is, verify that the spectrum analyzer shows only the expected output (as well as possible low-level harmonics of course). This should be done on a spectrum analyer that goes to at least 20 GHz or more, since our amplifiers could still have some gain at such frequencies. If there are other substantial magnitude spectral lines (other than harmonics) - you have stability problems that need to be fixed. If you do not see other spectral lines, try disconnecting the cable on the input and see if you see any outputs. Sometimes amplifiers will oscillate if their ports are not well terminated (in 50 Ohms)...

vi. Verify that the amplifier has reasonable gain, recording the value and comparing it with the expected gain from the datasheet and your simulations. NOTE: The signal generator and spectrum analyzer may each be off by as much as a dB each, and the interconnect cables could have a dB or more of loss, so don't expect exact gain values. Try to set up a good method to measure "insertion gain" to address these error sources. Discuss options with your classmates and instructor. Record/document your procedure and measurement results.

3. Compression Point Measurements

1) The amplifier input was specified as -20 dBm above since the amplifier gain will not be correct if it is "overdriven". In this part, we will find the critical input signal level where the gain begins to fall due to excess input signal power.

i. Slowly increase the signal input power in 1 or 2 dB steps. Record the output power versus input power in dBm until the gain falls by at least 1 dB from the value at low input levels. Record the input power at which this happens as the *1dB input-referred compression point*. You should ideally adjust for cable loss here. How does the compression point compare to the published value? Which is the data sheet using, input referred or output referred? (If output referred, divide by the gain to see what the data sheet thinks the input referred compression point should be ...

ii. Take additional data beyond the compression point until the output power does not increase any further . Typically you should go about 5 or 10 dB higher to see what the maximum output power is, assuming that is in the safe range. (***BUT - don't exceed the max allowed value at the input for the specific amplifier device or the maximum allowed output the test equipment can accept without damage !)***

iii. Plot your results (Pout vs Pin) in dBm and label the 1dB compression point - both input-referred on the horizontal axis and output-referred on the vertical axis. Also label the maximum output power.

4. Vector Network Analyzer (VNA) Measurement of S-Parameters

i. Using the instruction sheet near the VNA, set its output power to -20 dBm to prevent overdriving the amp. This typically involves setting the Port-1 attenuator in the unit to 20 dB.

ii. Set the frequency range to cover 40 MHz to 8 GHz (for the Advantest VNA), or 2 to 12 GHz (for the HP8510 VNA) .

iii. Calibrate the analyzer for measuring S21 using the cal-board's through path. Use the "response-cal" method. Then remove the cal board and put the amp in its place. IMPORTANT: Use the cal board that corresponds to your board type, and note where the reference-plane is. (how far in from the connector), so you know what location on your amplifier's input and output lines the impedance measurements correspond to.

iv. Measure and plot/photograph the amplifier gain (S21) graph in a log-magnitude dB format. Set a marker at your design frequency, record the gain value, and compare the measured value with the expected gain from the datasheet and from the previous measurement method. Is it reasonable, based on published values in the data sheet? How does it compare to the scalar measurement above? Discuss which may be more accurate and why and if you can't decide, discuss what your gain uncertainties are.

v. Next, calibrate for S11 using the 1-Port cal method and the cal board's SOL standards (as discussed in class). Then measure/plot the amplifier input impedance using Smith Chart format. *(Be sure to terminate port 2 in 50 Ohms during this measurement!)*

vi. Set the markers at various frequencies, print/plot/photograph the screen, and compare the measured values with those in the datasheet and/or S2P file.
vii. Turn your board around so that you are measuring S12 (isolation) and S22 (output reflection coefficient/impedance) and repeat.

2. Cascaded Amplifiers and Filters

i. Try cascading your amp with your partners' amp and measuring the overall gain. WARNING: You may need to use more than 20 dB attenuator setting to keep the input power low enough since the total cascaded gain may be more than 30 dB. Be sure to recalibrate if you change the attenuator setting.
ii. Why is the gain at low frequency so much higher than it is at your frequency of interest? (There could be multiple reasons)

3. Filter Testing

i. Build your filters designed in Part II and re-measure the board's S21 gain vs frequency.
ii. Connect the two boards in cascade and measure the overall cascaded amplifier response to see if the filters have helped concentrate the gain properly in your frequency range of interest.
iii. If you experience problems with stability, try adding a 3dB "pad" at the input to the amps. You could also try making your lambda/4 Vdd biasing line differently to make it more broadband. For example, place the biasing resistor at the junction between the output trace and the biasing line. See class discussion/notes for information on these topics.

Lab Writeup and Grading

As in earlier labs, you should turn in a combined report. However, *each person should write about half and each should document their own design and measurements (or at least coordinate in the writing of those parts).*

As always, be sure to provide explanations/discussions of your simulations, designs, construction, and measurement setups, values, and results. Graphics and photos are essential.

In describing your designs and measurements, your writeup should be detailed enough that another individual can understand what you did and could repeat it if necessary to check results.