BLOCK DIAGRAM

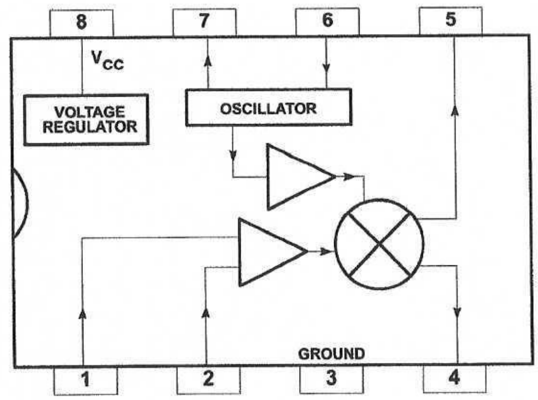

Figure 2. Block Diagram

AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS SA602A MIN	LIMITS SA602A TYP	LIMITS SA602A MAX	UNITS
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA602A is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the SA602A should be appropriately scaled.

Besides excellent low power performance well into VHF, the SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single ended output configurations and a balanced output.

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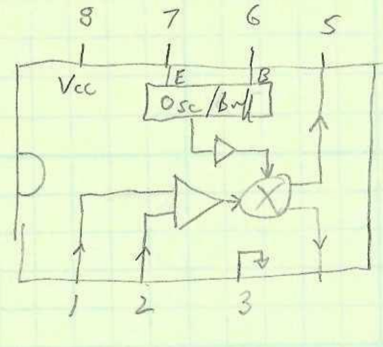
Signetics NE/SA 602 /612

Classic Example: ~~Overview of~~ NE 602:



TOP VIEW

Pass Out Data Sheet

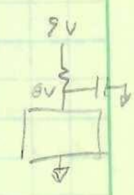
Pg 1

Read ~~Description~~
Features
...

Walk thru data sheet (pg 2) thru specs

Comment on ☆ Test Ckt ≠ Application Ckt

☆ max Voltage = 8V (To use 9V battery, do



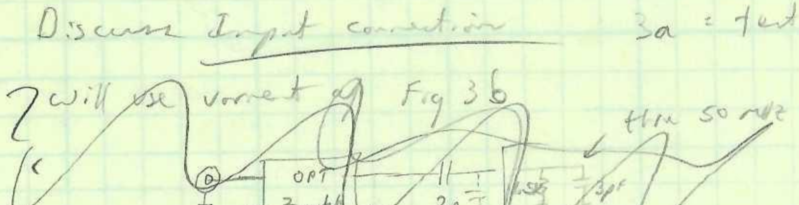
Describe purpose of each part of test ckt

Pg 3 Equivalent ckt ≠ actual e.g. Bias on Osc BUT
Shows enough to understand I/O constraints only
E.g. Pins 1 & 2 at some V, but must be AC coupled

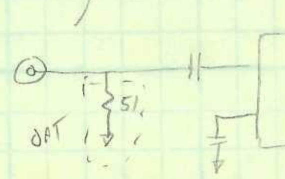
Discuss Input connection 3a = test ckt 3c vs (with 50Ω)

? will use variant of Fig 3b

thru 50 ohms?



Suggest initially



⇒ Gain decreased by 14dB $= 20 \log \sqrt{\frac{1.5k}{50}}$

i.e. Z match would step up voltage by $\sqrt{\frac{1500}{50}}$
(think about transformer match to see this

(pg 4)

Output Connection

Fig 4a — 155 kHz ceramic filter has $Z_{in} = 1.5\ k\Omega$
⇒ no matching needed

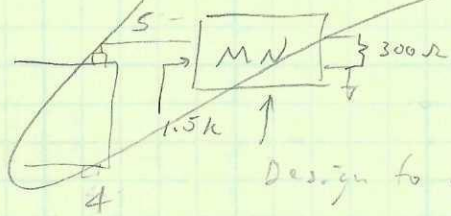
Fig 4b — Shows MNs (L networks w/ alignment)

4d — shows balanced (3 dB better gain)

20.5
− 3
17.5
15
2.5

~~USE SINGLE ended & MN to match to 300 Ω (will see next wk)~~

Let them choose



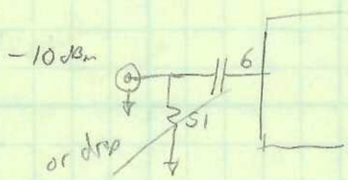
Design to be LOWpass

Osc

See discussion on pg 3 – can use external OSC input on 6
must be 200 mV peak-peak

⇒ 70 mV RMS
⇒ −10 dBm

If your osc puts out this, can do



(Pg 5) figures

(Pg 6) Discuss